Concept to Silicon

Available via Pure IP

NFP3112

Dual-Channel High Speed High Current Capability PIN Diode Driver

1. Device Features

- Dual channel
- ±5 V input control signals
- 3x3 mm QFN-16
- Also available in bare die form
- <30 ns rise / fall time at typical load
- Output range: -5 V to +5 V
- Other output voltage variants available

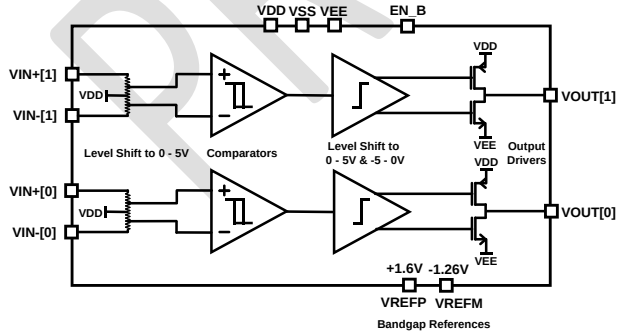
2. Device Applications

- RF PIN diode and switch control

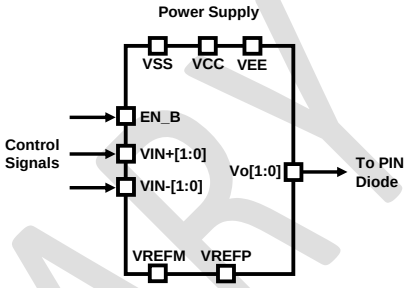
3. Device Description

The NFP3112x is a dual channel dual driver with dual polarity output capability. It is designed for switching PIN diodes with both fast rise and fall times, and sink / source capabilities.

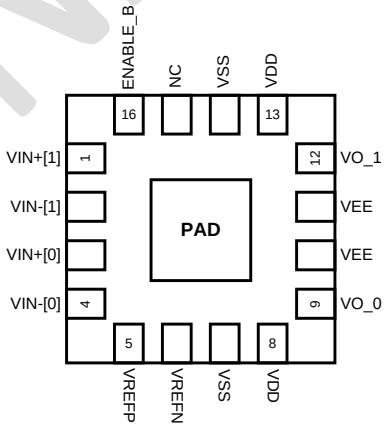
4. Simplified Block Diagram



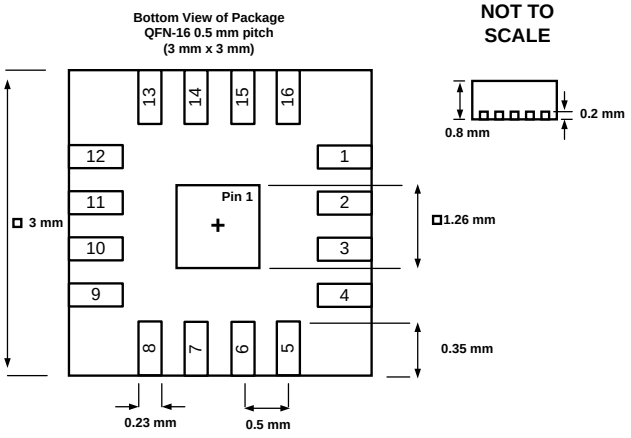
5. Simplified Application Diagram



6. Device Pin Out (Top View)



7. Package Description (Bottom View)



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8. Revision History

Table 1 – Revision History

Date	Version	Note
11/29/2021	0.02	Release of Draft
4/11/2022	0.03	Add V0.1 bare die information
4/13/2022	0.04	Add application schematic and corresponding measurement data

9. Pin Configurations and Functions

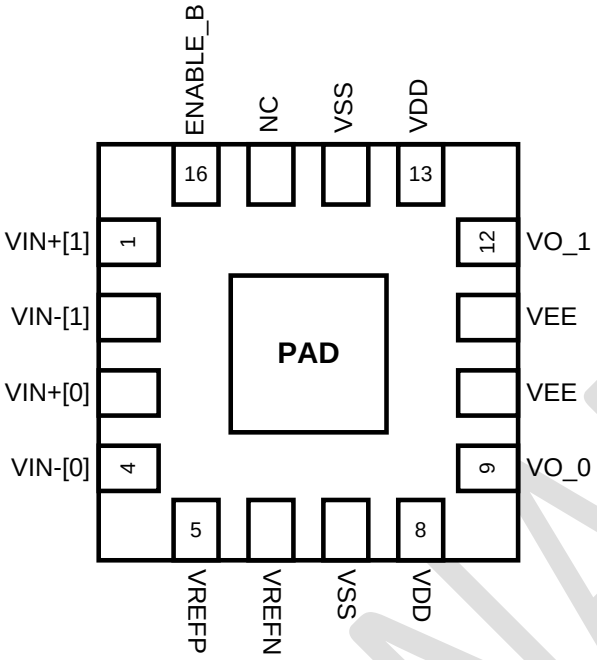

Figure 1 – Device Pinout

Table 2 – Pin Descriptions

PIN INFORMATION			Description
NAME	NO.	TYPE	
VIN+[1]	1	Analog Input	Analog input signal for channel 1 (positive side)
VIN-[1]	2	Analog Input	Analog input signal for channel 1 (negative side)
VIN+[0]	3	Analog Input	Analog input signal for channel 0 (positive side)
VIN-[0]	4	Analog Input	Analog input signal for channel 0 (negative side)
VREFP	5	Analog Output	Analog output for positive rail voltage reference (1.6 V)
VREFN	6	Analog Output	Analog output for negative rail voltage reference (-1.2 V)
VSS	7	Ground	Ground reference.
VDD	8	Power	Positive rail power supply.
VO[0]	9	Analog	Channel 0 analog output.
VEE	10	Power	Negative rail power supply.
VEE	11	Power	Negative rail power supply.
VO[1]	12	Analog	Channel 1 analog output.
VDD	13	Power	Positive rail power supply.
VSS	14	Ground	Ground reference.
NC	15	NC	No connect
ENABLE_B	16	Digital Input	Digital input for enabling drivers. Tie to ground for normal operation; tie to VDD to disable drivers.
PAD	PAD	Power	Connect to VEE

10. Specifications

10.1 Maximum Ratings

Table 3 – Maximum Ratings

Parameter	Description	Min	Typ	Max	Units
VIN_DIG	Digital Input voltage	-0.3		5.3	V
VIN	Analog Input voltage	-5.3		5.3	V
VOUT	Analog output voltage	-5.3		5.3	V
VCC	Positive rail supply voltage	-0.3		5.3	V
VEE	Negative rail supply voltage	-5.3		0.3	V
To	Operating temperature	-40		125	°C
Ts	Storage temperature	-40		85	°C

10.2 Electrical Characteristics

Table 4 – Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{VCC}	VCC supply current	VCC = +5V, VEE = -5V, $R_L = \infty$		13		mA
I_{VEE}	VEE supply current	VCC = +5V, VEE = -5V, $R_L = \infty$		8		mA
C_{IN}	Digital pin input capacitance			3.1		pF
V_{IL}	Digital input voltage low			0.876		V
V_{IH}	Digital input voltage high			1.084		V
R_{IN}	Signal Input Resistance	Resistance to VDD	9	10	11	kΩ
V_{OUTL}	Output voltage low	I_{OUT} = 100mA		VEE+0.5		V
V_{OUTH}	Output voltage high	I_{OUT} = 100mA		VCC-0.5		V
VDD	VDD operating range	VEE = -5V, I_{OUT} = 100mA	1.5	5	5.3	V
VEE	VEE operating range	VDD = +5V, I_{OUT} = 100mA	-2.8	-5	-5.3	V
V_{REFP}	Positive reference voltage	Measured from 0°C to 100°C	1.55	1.6	2	V
V_{REFM}	Negative reference voltage	Measured from 0°C to 100°C	-1.3	-1.26	-0.9	V

10.3 Output Timing

Table 5 – Output Timing Parameters

Parameter	Description	Conditions	Min	Typ	Max	Units
$T_{D\ RISE}$	Rising propagation delay	VCC = +5V, VEE = -5V, $R_L = \infty$		5		ns
$T_{D\ FALL}$	Falling propagation delay	VCC = +5V, VEE = -5V, $R_L = \infty$		6		ns
T_{RISE}	Output rise time	VCC = +5V, VEE = -5V, $R_L = \infty$		15	20	ns
T_{FALL}	Output fall time	VCC = +5V, VEE = -5V, $R_L = \infty$		15	20	ns
T_{RISE}	Output rise time under load	VCC = +5V, VEE = -5V, R_L = 50Ω, C_L = 1nF		30		ns
T_{FALL}	Output fall time under load	VCC = +5V, VEE = -5V, R_L = 50Ω, C_L = 1nF		30		ns

11. Detailed Description

11.1 Overview

This chip is a dual-channel dual rail output driver intended for driving PIN diodes in RF front end systems. Using the digital inputs, the output voltage switches from VEE to VCC with short transition times to forward and reverse bias the PIN diode load.

11.2 Features

- Small QFN package
- Dual channel
- Dual polarity rail

11.3 Block Diagram

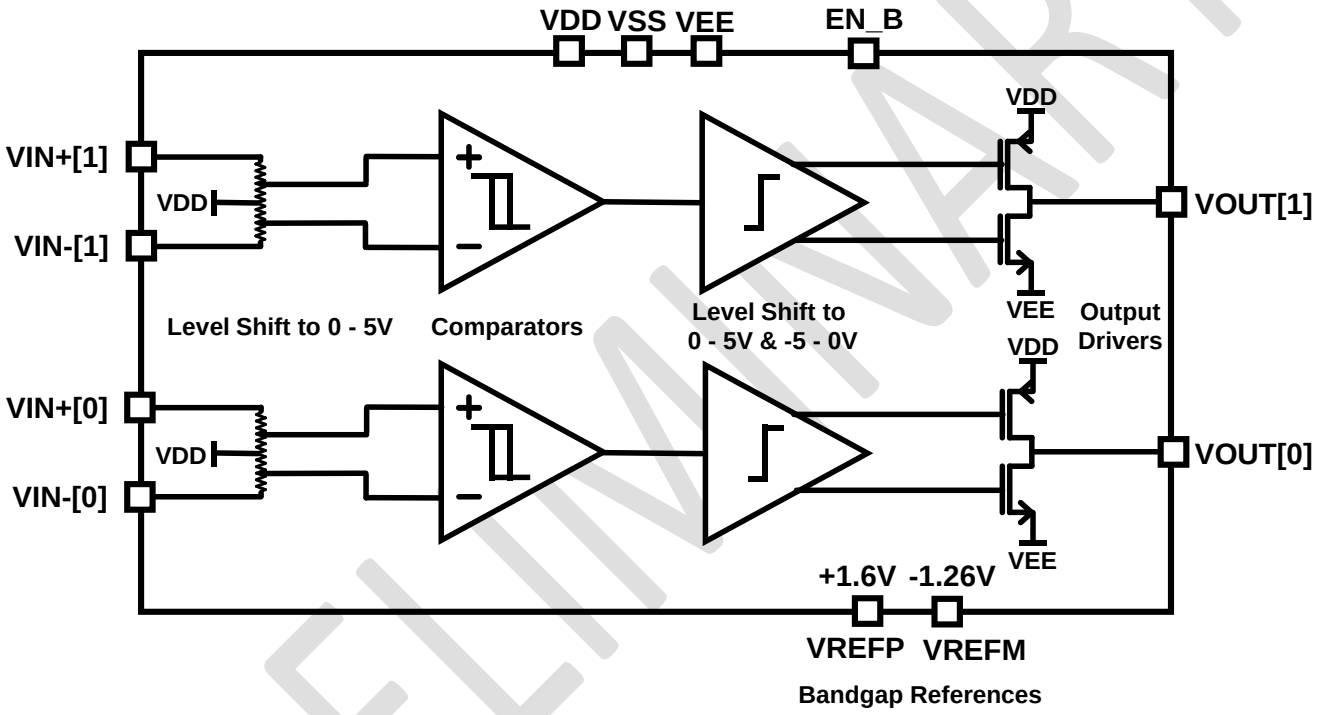

Figure 2 – Block Diagram

12. Application and Implementation

Note

Information in this section is not part of NFR's device specification. Accuracy and completeness are not warranted by NFR. NFR's customers are solely responsible for determining whether the device is appropriate for their applications. Customers should characterize and verify their design and systems to confirm functionality.

12.1 Application Schematic

Below is an application schematic demonstrating configuration of supply ballast resistors. The ballast resistors prevent chip damage during overcurrent events.

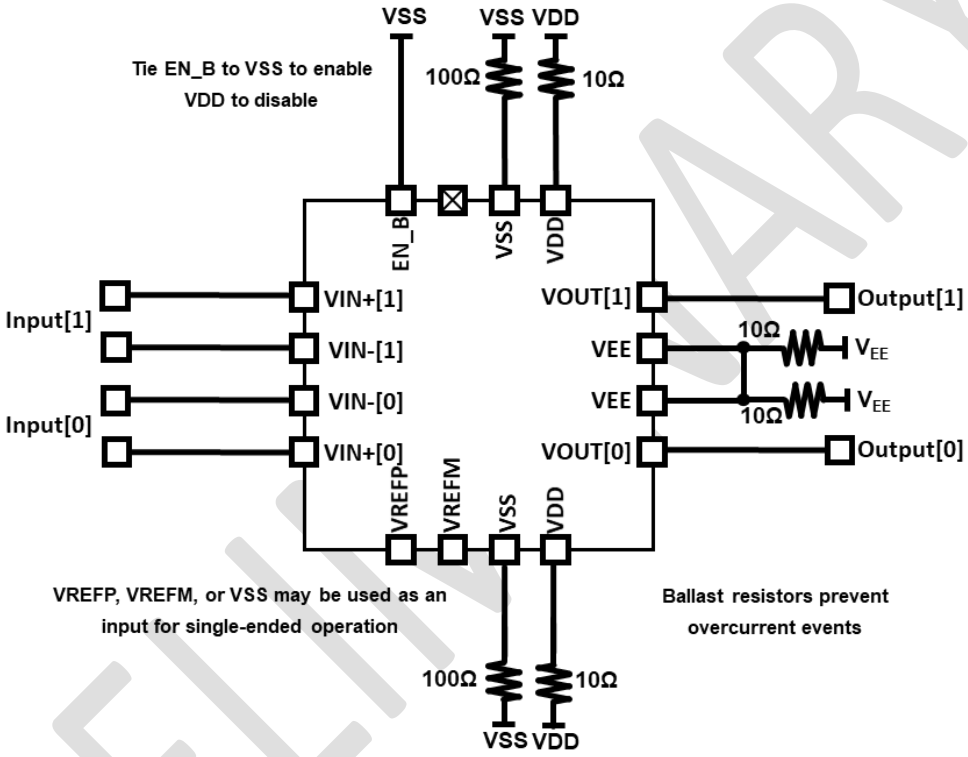

Figure 3 – Application Schematic

12.2 Typical Output Waveforms

Below are typical output waveforms (blue) with annotated rise and fall time, along with associated input waveforms (yellow). Measurements were performed set up as shown in the application schematic in Figure 4. The output is driving a load of 50Ω in parallel with 1nF.

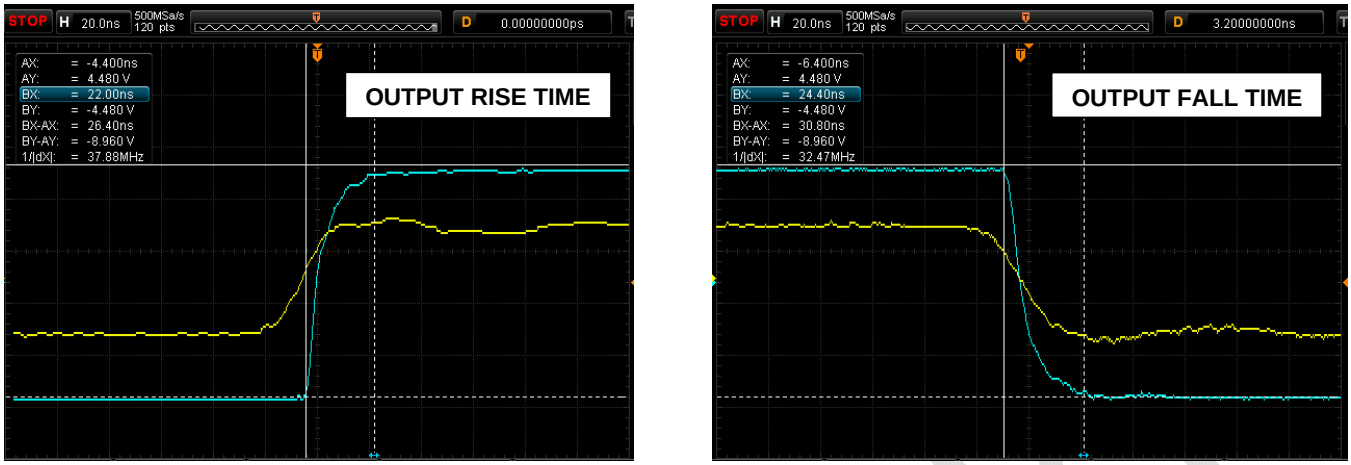

Figure 4 – Output Waveforms

13. Power Supply and Sequencing Recommendations

13.1 Power Supply Decoupling Recommendation

For power supply decoupling, the recommendation is to have at minimum a 1 µF bulk capacitance between the VDD and VSS rails, and between the VDD and VEE rails. An additional 1 nF capacitor with low ESR on each rail pair reduces voltage ripple during fast transient events.

13.2 Power Supply Sequencing Recommendation

For power supply sequencing, the recommendation is to ensure VDD is powered on first, and powered off last as the digital inputs of the chip is powered by VDD. Following that it's recommended to power on VEE, then VCC. The recommended power off sequence is the reverse of the power on sequence (*i.e.* last supply turned on should be first supply turned off).

14 Layout Guidelines

Best practices should be followed when laying out the PCB for the chip:

1. Placement of decoupling caps close to the chip, minimizing parasitic components.
2. Sufficiently wide traces to reduce IR drops or parasitic inductive elements.

Chip will be available in both die and QFN packaged forms.

15. ESD Info

All power supplies and I/Os have ESD structures associated with their output voltage range and corresponding power rails. Best practices should be followed when handling the chip either manually or with machines.

16. Device Package Information

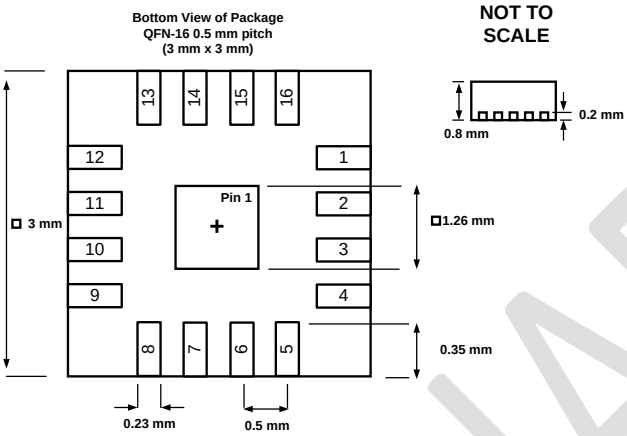

Figure 5 – Device Packaging Diagram

17. Bare Die Dimensions

The bare die is 1050 μm by 1200 μm. Pad openings are all 100 μm by 100 μm. Pad center locations relative to chip center are given in Table 6.

Figure 6 – Scale diagram of NFP3112 bare die pads. Overall dimensions are 1050 μm by 1200 μm

PAD	X (μm)	Y (μm)
EN_B	-448	520
VIM1	-448	316
VIP1	-448	112
VIP0	-448	-92
VIM0	-448	-296
VREFP	-448	-500
VREFM	-244	-523
VSS2	-40	-523
VDD1	263	-381
VOUT0	263	-177
VEE	263	27
VOUT1	263	231
VDD1	-32	385
VSS1	-240	385

Table 6 – Pad center locations relative to chip center

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