Bringing Array Front-End Control to the Edge

GaN Amplifier Controlled by Highly Integrated Bias Voltage Controller

White Paper

NoiseFigure Research
www.noisefigure.com
hello@noisefigure.com

NFR
Concept to Silicon

Abstract

This white paper highlights the usage of an ultra-compact IC from NFR that allows GaN amplifier bias control to be brought physically close to the RF front end elements in an array. A high-efficiency C-band GaN-on-SiC HEMT power amplifier (QPA1019) by Qorvo is used together with an NFR bias voltage controller IC (NFP4002) to demonstrate a 2-chip solution. The two stage GaN power amplifier (PA) achieves greater than 10-W output power and 39% Power Added Efficiency (PAE) at 22 V bias from 4.5 to 7.0 GHz, with 19-dB large-signal gain, and suppressed second harmonic output. The PA's biasing and sequencing needs are provided by the NFP4002. Test results show no difference in RF performance when comparing the bias voltage controller setup versus a testbench with 3 power supplies. Furthermore, the NFP4002 demonstrates short drain voltage transition times (< 16 ns) to meet stringent pulsed system timing requirements.

Introduction

GaN amplifier biasing typically requires high drain voltage handling capability, and the ability to provide negative voltages for gate control. Additionally, proper sequencing of voltages is of importance to ensure the amplifier is not damaged. In application, these high-performance amplifiers may be used as part of a TRM (Transmitter Receiver Module) in single channel or multi-channel phased array architectures. NFR's family of bias voltage controllers is developed to support biasing of such devices in high-density environments by providing digitally controlled timing of PA drain, T/R switch, and gate biasing voltages to single or multi-stage amplifiers, or PA/LNA combination transceiver modules. In addition, to aid in system integration, tuning of individual output's timing, sensing, and protection are all included and accessed with a SPI protocol that's scalable to the specific size of the system.

Test Information

Two biasing schemes for the QPA1019 10-W amplifier were tested, per Figure 1 and 2 below, and the results were compared. Control parameters are entered via PC software and sent through the SPI bus connected to the NFP4002. The chip turns on the negative polarity voltages at the gate terminal prior to enabling the drain voltages, providing proper bias sequencing. When the NFP4002 chip is triggered using the PC software, the NFP4002 switches the drain output voltage levels from 0 to 22 V. NFP4002's gate bias voltage outputs can be configured in increments of 10 mV.

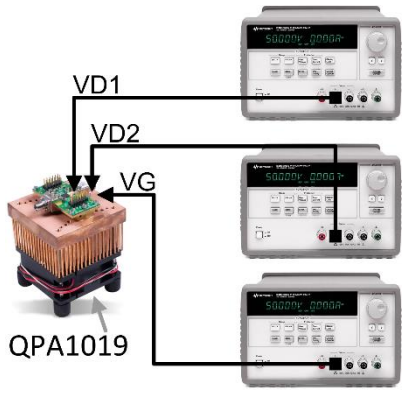

Figure 1 – QPA1019 setup without NFR bias voltage controller. Note: VG1 is biased at -2.44 V. VD1 and VD2 range from 0 V for disabling and 22 V for enabling the amplifier.

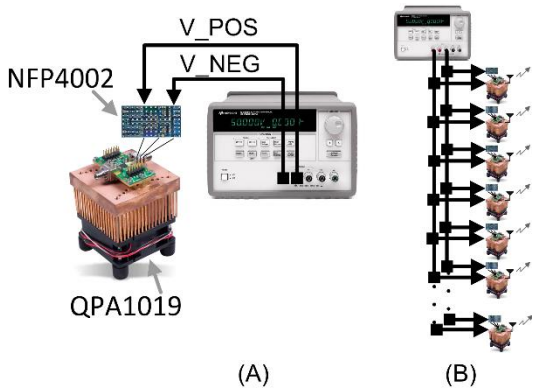

Figure 2 – (A) QPA1019 setup with NFR bias voltage controller NFP4002. (B) Sample system diagram using the 2-chip solution with biasing at the edge. NOTE: the same biasing voltages are used as in Figure 1. This time provided by the NFP4002.

Test Results

Figure 3 below shows the PA's Pout (dBm) versus Pin (dBm) measured at 5.8 GHz and 22 V bias, with no distinguishable differences when comparing the two setups, demonstrating that the controller IC provides perfect biasing conditions for the. When scaling the setup to a larger number of amplifiers, setup 2 (shown in Figure 2) provides the distinct benefits of being able to digitally control individual amplifiers, fitting everything at the front end near each antenna element, monitoring the health of each element, and enabling high PRF (Pulse Repetition Frequency) applications. The drain current is monitored constantly to a customizable limit such

that in the event of an overcurrent condition, the drain voltage is quickly shut off to protect the amplifier and system. Furthermore, when used in a large system, the bias point of each FET stage or amplifier may be tuned to optionally compensate for differences in temperature, device variation, or effects of semiconductor lifetime. Figure 4 illustrates the transient drain voltage rise time to be 15.4 nanoseconds.

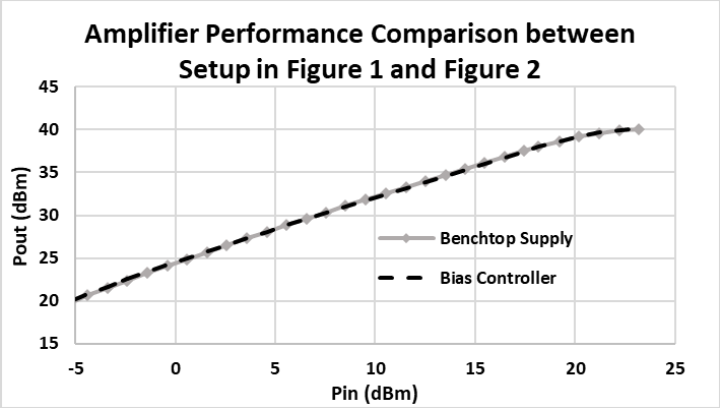

Figure 3 – Amplifier Pout Comparison between traditional biasing and NFR controller

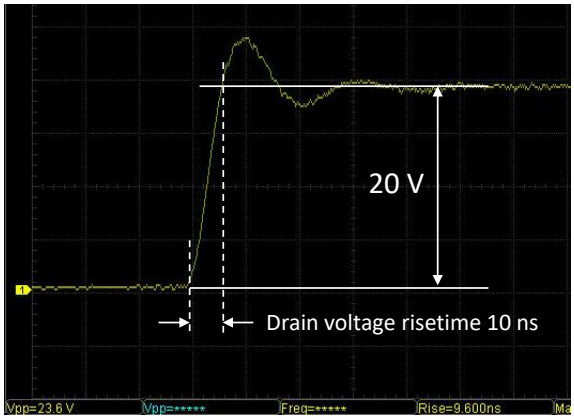

Figure 4 – ~10 ns PA Drain Voltage Rise Time with 33 Ohm and 2 nF load

Contact

To learn more, email hello@noisefigure.com to request further details about the NFR NFP4002.

About

NFR, located in Renton, Washington, is a team of semiconductor designers and product inventors. NFR has taped out ASICs using process nodes from 1µm to 14nm and has global supplier partnerships for manufacturing, packaging, and testing to deliver first prototypes and volume production chips to customers. NFR's products are used across Defense, Commercial, and Aerospace industries.